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| 09/716,493 | 11/20/2000 | Gilbert Laurenti | TI-30026 | 8620 |

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| EXAMINER | |
|---|---|
| O'BRIEN, BARRY J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 5 |

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/716,493 | LAURENTI ET AL. | |
| | Examiner | Art Unit | |
| | Barry J. O'Brien | 2183 | |

*-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 November 2000, 23 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. Claims 1-11 have been examined.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Information Disclosure Statement as received on 11/20/2000 and Declaration as received on 4/23/2001.

### *Priority*

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in France on March 10, 2000. It is noted, however, that applicant has not filed a certified copy of the Application No. 00400687.0 as required by 35 U.S.C. 119(b).

### *Drawings*

4. The drawings are objected to because of the following:

a. Figure 1 has reference numeral 104 labeled as a "memory management unit", while the specification on page 7 line 19 recites reference numeral 104 as "memory interface unit". Please correct the drawing to have a label consistent with the specification.

b. Figure 1 has reference numeral 22 labeled as a "ASIC Backplane", while the specification on page 7 line 22 recites reference numeral 22 as "backplane bus". Please correct the drawing to have a label consistent with the specification.

5. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

7. The disclosure is objected to because of the following informalities:

a. Page 6 lines 13 and 16 refer to Fig.1 reference number 100 as a "processor". However, on lines 19 and 26 reference number 100 is referred to as "microprocessor". Please correct to be consistent with one naming convention.

Appropriate correction is required.

***Claim Objections***

8. Claim 1 is objected to because of the following informalities:

a. Regarding claim 1, please insert the word "to" before the phrase "operable inhibit" on the second to last line of the claim so that the claim reads more clearly.

9. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Favor et al, U.S. Patent No. 5,649,137.

12. Regarding claim 1, Favor has taught a digital system comprising a microprocessor (10 of Fig.1), wherein the microprocessor comprises:

a. An execution unit (17 of Fig.1);

b. Memory interface circuitry (see 25 of Fig.1) operable to fetch an operand from memory and to provide the operand to the execution unit (see Col.6 lines 9-16);

c. Address pointer circuitry (32 of Fig.1) operable to provide an address of the operand to the memory interface circuitry (see Col.6 lines 9-16 and 23-25);

d. Modification tracking circuitry connected to the address pointer circuitry, the modification tracking circuitry operable to inhibit a redundant fetch of the operand (see Col.4 lines 12-20 and Col.6 lines 9-16).

13. Regarding claim 4, Favor has taught claim 1 as shown above, wherein the execution unit (17 of Fig.1) is a multiply-accumulate (MAC) unit (see Col.5 lines 64-67).

*Claim Rejections - 35 USC § 103*

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Favor et al, U.S. Patent No. 5,649,137 as applied to claim 1 above.

16. Regarding claim 2, Favor has taught claim 1 as shown above, further comprising a data cache (35 of Fig.1) to hold the operand prior to use by the execution unit, with an address pointer to the data (see Col.6 lines 22-25). Favor has not taught that the data cache be a shadow register.

17. However, a shadow register is defined in the art as a secondary copy of data, generally a copy of data that exists in memory already, and is fetched for use by the execution unit. One of ordinary skill in the art would have recognized that a data cache will function at sizes from one entry to an extremely large number of entries, varying in performance and cost due to size of the cache. Regardless of the number of entries, the cache will check for an address hit, and thus if there is only one entry, then only one address comparison must be made. Also, it is well known in the art that reducing the cost of hardware is a paramount concern of microprocessor design. Therefore, one of ordinary skill in the art would have found it obvious to modify the data cache to be one entry and function as a shadow register, containing a copy of data which already exists in, and has been fetched from, memory, and which is addressed by a pointer, in order to reduce the amount of hardware needed by the cache, and thus reducing the cost to manufacture the hardware.

18. Regarding claim 9, Favor has taught a method of operating a digital system comprising a microprocessor (10 of Fig.1), comprising the steps of:

a. Loading a data pointer with a first address value. While not taught explicitly, it is inherent that in a system with a cache that data is loaded into it before execution, and because the cache contains an address field, that the data be an address (see Col.6 lines 9-16 and 23-25).

b. Executing a first instruction in the microprocessor that requires at least a first operand from memory in accordance with the data pointer by fetching the first operand from memory in accordance with the first address value (see Col.4 lines 12-20);

c. Executing a second instruction in the microprocessor that requires at least a second operand from memory in accordance with the data pointer by inhibiting fetching of the second operand from memory if the address of the second operand is not in the cache (see Col.4 lines 12-20).

19. Favor has not taught that fetching is inhibited if the value of the data pointer has not been modified since the step of executing the first instruction.

20. However, it is well known in the art that a data cache contains an address pointer and the data pointed to by that pointer, and before execution an address is checked against the addresses in the cache in an attempt to find a hit. Furthermore, one of ordinary skill in the art would have recognized that a data cache will function at sizes from one entry to an extremely large number of entries, varying in performance and cost due to size of the cache. Regardless of the number of entries, the cache will check for an address hit, and thus if there is only one entry, then only one address comparison must be made. Also, it is well known in the art that reducing the cost of

hardware is a paramount concern of microprocessor design. Therefore, one of ordinary skill in the art would have found it obvious to modify the data cache to be one entry and function as data pointer which will then, because of its caching properties, only inhibit fetching of the operand from memory if the one address in the cache is unchanged since the last instructions execution, reducing the amount of hardware needed by the cache, and consequently reducing the cost to manufacture the hardware.

21. Regarding claim 10, Favor has taught the method of claim 9, wherein the step of executing the first instruction comprises loading the first operand into a cache, such that during the step of executing the second instruction the cache is not reloaded with the same operand if there is a cache hit (see Col.4 lines 12-20).

22. Favor has not taught the loading of the first operand into a non-accessible shadow register, and that during the execution of the second instruction the shadow register is not reloaded if the data pointer has not been modified since the step of executing the first instruction.

23. However, a shadow register is defined in the art as a secondary copy of data, generally a copy of data that exists in memory already, and is fetched for use by the execution unit. One of ordinary skill in the art would have recognized that a data cache will function at sizes from one entry to an extremely large number of entries, varying in performance and cost due to size of the cache. Regardless of the number of entries, the cache will check for an address hit, and thus if there is only one entry, then only one address comparison must be made. Also, it is well known in the art that reducing the cost of hardware is a paramount concern of microprocessor design. Therefore, one of ordinary skill in the art would have found it obvious to modify the data cache to be one entry and function as a shadow register, containing a copy of data which already exists

in, and has been fetched from, memory, and which is addressed by a pointer, reducing the amount of hardware needed by the cache, and thus reducing the cost to manufacture the hardware.

24. Furthermore, it is well known in the art that a data cache contains an address pointer and the data pointed to by that pointer, and before execution an address is checked against the addresses in the cache in an attempt to find a hit. One of ordinary skill in the art would have recognized that a data cache will function at sizes from one entry to an extremely large number of entries, varying in performance and cost due to size of the cache. Regardless of the number of entries, the cache will check for an address hit, and thus if there is only one entry, then only one address comparison must be made. Also, it is well known in the art that reducing the cost of hardware is a paramount concern of microprocessor design. Therefore, one of ordinary skill in the art would have found it obvious to modify the data cache to be one entry and function as data pointer which will then, because of its caching properties, only inhibit fetching of the operand from memory and loading single cache entry if the one address in the cache is unchanged since the last instructions execution, reducing the amount of hardware needed by the cache, and consequently reducing the cost to manufacture the hardware.

25. Regarding claim 11, Favor has taught the method of claim 9, further comprising:

a. The step of loading the cache with a second address value between the step of executing the first instruction and the step of executing the second instruction. While not taught explicitly, it is inherent that when there is a cache miss and data is fetched from memory that it will be written into the cache at a an address not in the cache previously, otherwise there would have been a cache hit (see Col.4 lines 12-20).

b. Wherein the step of executing the second instruction comprises fetching the second operand from memory in accordance with the second address value (see Col.4 lines 12-20).

26. Favor has not taught that the cache be a data pointer. However, it is well known in the art that a data cache contains an address pointer and the data pointed to by that pointer, and before execution an address is checked against the addresses in the cache in an attempt to find a hit. One of ordinary skill in the art would have recognized that a data cache will function at sizes from one entry to an extremely large number of entries, varying in performance and cost due to size of the cache. Regardless of the number of entries, the cache will check for an address hit, and thus if there is only one entry, then only one address comparison must be made. Also, it is well known in the art that reducing the cost of hardware is a paramount concern of microprocessor design. Therefore, one of ordinary skill in the art would have found it obvious to modify the data cache to be one entry and function as data pointer which will then, because of its caching properties, fetch the second operand from memory if there is a cache miss, reducing the amount of hardware needed by the cache, and consequently reducing the cost to manufacture the hardware.

27. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Favor et al, U.S. Patent No. 5,649,137 as applied to claim 1 above, and further in view of Whitley, U.S. Patent No. 4,531,200.

28. Regarding claim 3, Favor has taught claim 1 as shown above, but has not taught wherein the address pointer circuitry is a stand-alone coefficient data pointer.

29. However, Whitley has taught an indexed indirect addressing mode which uses a base register combined with an index value to address data structures such as lists, queues, and stacks, efficiently (see Col.1 lines 10-23). Because a coefficient data pointer is defined as a memory mapped register (p.22 of applicant's specification), one of ordinary skill in the art at the time of the invention would have found it obvious to implement the indexed indirect addressing mode using a register in the DTAG Chip (32 of Fig.1 of Favor), which contains an address (see Col.6 lines 23-25 of Favor) as a coefficient data pointer in order to index into various data structures more efficiently.

30. Regarding claim 7, Favor has taught claim 1 as shown above, but has not taught wherein coefficient data pointer modification tracking circuitry is operable to only track pointer modification during looping operations of the microprocessor.

31. However, Whitley has taught the use of indexed indirect addressing which is used in accessing sequential elements in data structures such as lists and queues (see Col.1 lines 10-22), but the method of addressing has associated overheads (see Col.1 lines 23-25). One of ordinary skill in the art would have recognized that sequentially addressed elements of a data structure are generally accessed sequentially by adding an incremented value to a base pointer (see Col.1 lines 12-16), such as in a stack pointer, and the incrementing and subsequent accessing are performed during branching operations, such as popping elements on/off a stack when switching contexts. Therefore, one of ordinary skill in the art would have found it obvious to only enable the modification tracking circuitry as described by Favor above during branching or looping accesses to data structures so as to minimize the overhead associated with the indexed indirect

addressing mode that is used when accessing sequential data structure elements via a base pointer.

32. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Favor et al, U.S. Patent No. 5,649,137 as applied to claim 1 above, and further in view of Schacham et al, UK Patent Application GB2200481A.

33. Regarding claim 5, Favor has taught claim 1 as shown above, but has not explicitly taught wherein a touch instruction "mar(*CDP)" is provided to flag that the operand has been updated in the memory circuit so that the updated operand can be fetched for use by the execution circuit.

34. However, Favor has taught that when there is a cache hit during a write instruction that the cache line is invalidated so that the entry is re-fetched from memory the next time it is accessed (see Col.18 lines 60-67), the method being performed in hardware. One of ordinary skill in the art would have recognized the need to maintain a level of coherency between a memory and a cache located near to the execution unit, and that the enforcement of this policy can be carried out in hardware or by the user in software. Also, it is well known in the art that reducing the cost of hardware is a paramount concern of microprocessor design. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to implement a cache coherency protocol automatically in software by executing an instruction which performs the same operation as Favor's hardware does, thereby eliminating some hardware and thus reducing the cost to manufacture it.

35. Conversely, the claim language can be interpreted to be a specific instruction, rather than simply the process as shown above, to invalidate an operand in a cache. In this case, Favor has

not taught a touch instruction to flag the operand that has been modified so it can be fetched again.

36. Schacham has taught a cache invalidation instruction which can be executed to invalidate a cache so that operands are forced to be re-fetched (see p.4 lines 28-32). One of ordinary skill in the art would have recognized that for the best performance and correct operation, a cache must contain the most up-to-date information in relation to the main memory (see p.2 lines 8-23), and that ensuring that the correct data is in the cache can be implemented in hardware or by the user in software. Furthermore, there can be problems such as extra hardware needed and address bus contention on the cache if the implementation is carried out in hardware (see p.3 lines 1-13). Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to use a cache invalidate instruction to invalidate operands in a cache, thereby forcing their re-fetching and ensuring the correct data is available for execution.

37. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Favor et al, U.S. Patent No. 5,649,137 as applied to claim 1 above, and further in view of Okabayashi et al, U.S. Patent No. 6,505,309.

38. Regarding claim 6, Favor has taught claim 1 as shown above, but has not taught wherein an override mechanism is provided to disable the modification tracking circuitry.

39. However, Okabayashi has taught the disabling of cache circuitry during a debugging process in order to test if correct sequences of instructions are executed (see Col.1 lines 19-34). One of ordinary skill in the art would have recognized that it is desirable to be able to debug the execution of instructions in a processor separately from the memory and caching systems so that problems can be more accurately located. Because the modification tracking circuitry of Favor

is located within a cache (see Col.4 lines 12-20 and Col.6 lines 9-16 of Favor), one of ordinary skill in the art at the time of the invention would have found it obvious to provide a mechanism to disable the cache for debugging purposes.

40. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Favor et al, U.S. Patent No. 5,649,137 as applied to claim 1 above, and further in view of Willkie et al., U.S. Patent No. 5,923,705.

41. Regarding claim 8, Favor has taught the digital system according to Claim 1 as shown above, but has not taught the digital system being a cellular telephone.

42. Wilkie has taught a cellular telephone (14 of Fig.1) further comprising:

a. An integrated keyboard connected to the processor via a keyboard adapter (see Fig.1);

b. A display, connected to the processor via a display adapter (see Fig.1);

c. Radio frequency (RF) circuitry connected to the processor (see Fig.2);

d. An aerial connected to the RF circuitry (see Fig.1).

43. One of ordinary skill in the art would have recognized that modern cellular phones require a processor to process digital data and voice signals that are received and transmitted from the phones (see Willkie Col.1 lines 15-20 and 28-31). Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to use the processor (Favor, 10 of Fig.1) in a cellular telephone digital system to process digital data and voice signals.

***Conclusion***

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

45. Burky et al, U.S. Patent No. 6,275,918, has taught a method for pre-fetching operands from memory using a pre-fetch history table.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
10/1/2003

EDDIE CHAN
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